Kingston DDR3/3L DRAM for embedded applications

Kingston DDR3/3L

Kingston on-board DRAM is designed to meet the needs of embedded applications and offers a low-voltage option for lower power consumption.

DDR3/3L Part Numbers and Specifications

30nm DDR3/3L Part Number	Capacity	Description	Package Size	Configuration (words x bits)	Speed	VDD, VDDQ	Operating Temperature
D1216ECMDXGJD	2Gb	96 ball FBGA DDR3/3L I-Temp	7.5x13.5x1.2	128Mx16	1866 Mbps	1.35V	0°C ~ +95°C
D2568ECMDPGJD	2Gb	78 ball FBGA DDR3/3L I-Temp	7.5x13.5x1.2	256Mx8	1866 Mbps	1.35V	0°C ~ +95°C
D2516ECMDXGJD	4Gb	96 ball FBGA DDR3L	7.5x13.5x1.2	256Mx16	1866 Mbps	1.35V*	0°C ~ +95°C
D5128ECMDPGJD	4Gb	78 ball FBGA DDR3L	7.5x10.6x1.2	512Mx8	1866 Mbps	1.35V*	0°C ~ +95°C
D2516ECMDXGME	4Gb	96 ball FBGA DDR3L	7.5x13.5x1.2	256Mx16	2133 Mbps	1.35V*	0°C ~ +95°C

*Backward compatible to 1.5V VDD, VDDQ
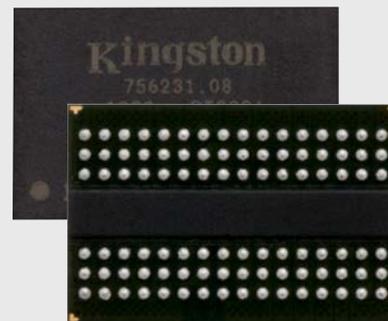
Key Features

- Double-data-rate architecture: two data transfers per clock cycle

- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture

- Bi-directional differential data strobe (DOS and /DQS) is transmitted/received with data for capturing data at the receiver

- DOS is edge-aligned with data for READS; center-aligned with data for WRITES

- Differential clock inputs (CK and /CK)

- DLL aligns DQ and DOS transitions with CK transitions

- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS

- Data mask (DM) for write data

- Posted /CAS by programmable additive latency for better command and data bus efficiency

- On-Die Termination (ODD for better signal quality
  — Synchronous ODT
  — Dynamic CDT
  — Asynchronous ODT

- Multi Purpose Register (MPR) for pre-defined pattern read out

- ZQ calibration for DO drive and ODT

- Programmable Partial Array Self-Refresh (PASR)

- RESET pin for Power-up sequence and reset function

- SRT range: Normal/extended

- Programmable Output driver impedance control